

PHASE I REPORT ON
DEVELOPMENT OF A LOW-NOISE
8 mm RECEIVER FRONT END

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TRG Incorporated
A Subsidiary of Control Data Corporation
Route 110
Melville, L.I., New York

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ABSTRACT

A low noise, wide-band receiver front end in the 8.5 mm (35 Gc) region is being developed by TRG, Melville, N.Y. for Jet Propulsion Laboratory, Pasadena, California. This report summarizes the findings of the Developmental Phase, (Phase I) of the program and makes recommendations for the Final Phase (Phase II).

This report, prepared in accordance with the contract, summarizes the findings of the development phase (Phase I) of a program to provide a low-noise, wide-band receiver front-end for radio astronomy purposes in the 8.5 mm (35 Gc) region.

Under this program, two types of amplifier design have been evaluated for maximum Survey Range. The first type utilizes a single diode in split waveguide, and the second, a balanced diode configuration with the bias applied through the coaxial idler circuit. The single-diode split-waveguide mount is shown in Figs. 1 and 2. The diode chip, mounted inside 6 mil high waveguide, is biased with a gold mesa contacting ribbon. Spring tension insures firm electrical contact. Electrical tests on the split waveguide mount showed that some idler circuit tuning could be achieved by adjusting the length of the ribbon. With this idler circuit the amplifier exhibited 15 db gain with a 200 Gc instantaneous bandwidth and was tunable across a 2 Gc frequency range. This amplification, achieved with an excessive amount of pump power (200 mw), indicated the need for gold plating the substrate of the diode chip used. The tuning range of the diode mount is limited by diode quality and should improve as better quality diodes become available.

The balanced integrated amplifier is shown in Figs. 3 and 4. In this mount the idler circuit has an accessible coaxial port which is used for tuning and biasing the diodes. Recent tests on the balanced mount have shown a tuning range of 4 Gc with a gain of 20 db and an instantaneous bandwidth of 100 Mc. This performance, encouraging as an initial step, can be improved with further engineering effort. Development of the full bandwidth and gain capabilities of both mounts has not yet been realized because of the delayed delivery of diode chips from Sylvania.

Delays in delivery of high quality varactor chips have caused a reorientation in the proposed program for Phase II. Originally, it was assumed that all development of the amplifier would be completed at the end of Phase I. Instead there has been partial development of two designs with the balanced diode mount design appearing somewhat more promising.

During Phase II, the present balanced diode mount, though not yet complete, would be integrated into the cooled system with parallel engineering effort directed toward improving its electrical performance.

Noise figure measurements on the mount are considered premature at the present time and will not be made until Phase II is underway. Losses in waveguide runs and choke joints to be developed during Phase II are to be considered in the overall noise figure budget.

Discussion of Contract Provisions

Section 2.22 requires that all system specifications be met within two hours after turn on. Using the A. D. Little cryogenic refrigerator discussed in the proposal, cooling down the amplifier mass to 20°K will probably take about 3 hours.

Section 3.1 specifies the maximum package dimensions of 20" diameter and 20" length. The proposed A. D. Little Model 340LS refrigerator is, in fact, the only suitable commercial refrigerator for the project, but it will not meet the 20" overall length requirement. It is estimated that an overall package length of 28" can be achieved with the A. D. Little refrigerator, as shown in Fig. 5.

Finally, the contract calls for completion of Phase II by Dec. 24, 1966. JPL is aware of the program delays TRG has had in obtaining suitable diodes, and that contract funds were carefully conserved. This delay in obtaining suitable diodes will extend the proposed delivery schedule by approximately three (3) months. However, present contract funds should be sufficient to complete the program.

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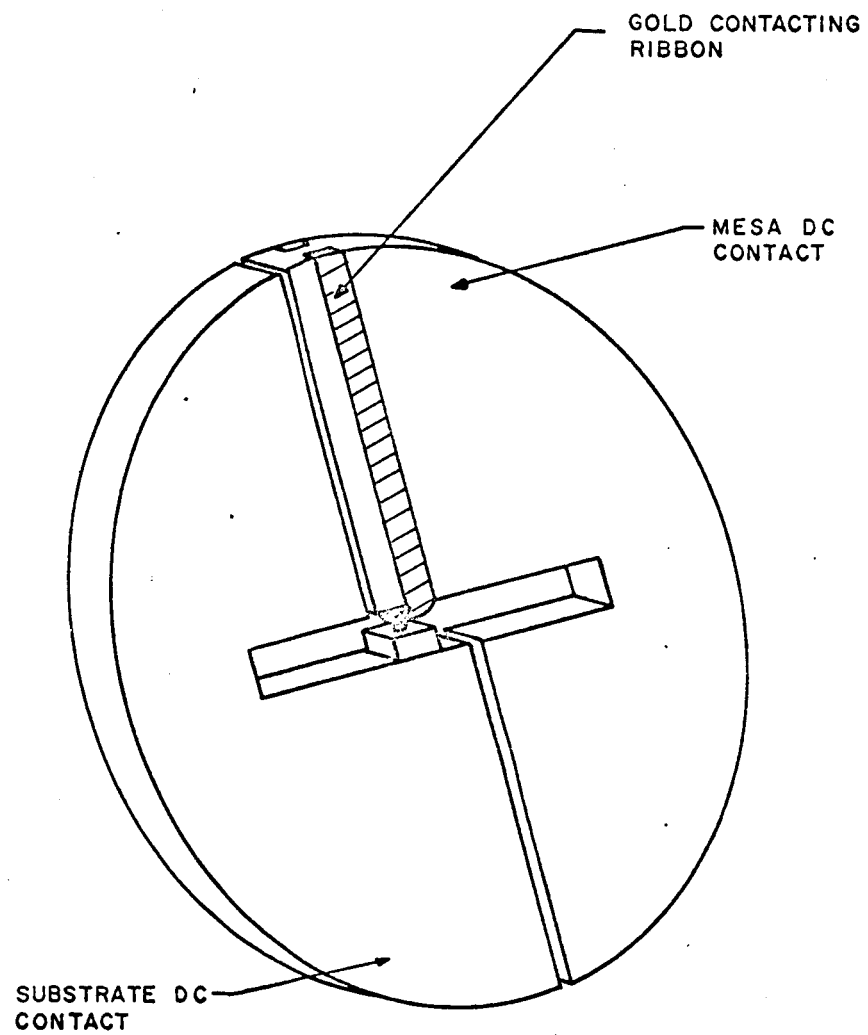


FIGURE 1. DIODE MOUNTED IN SPLIT WAVEGUIDE

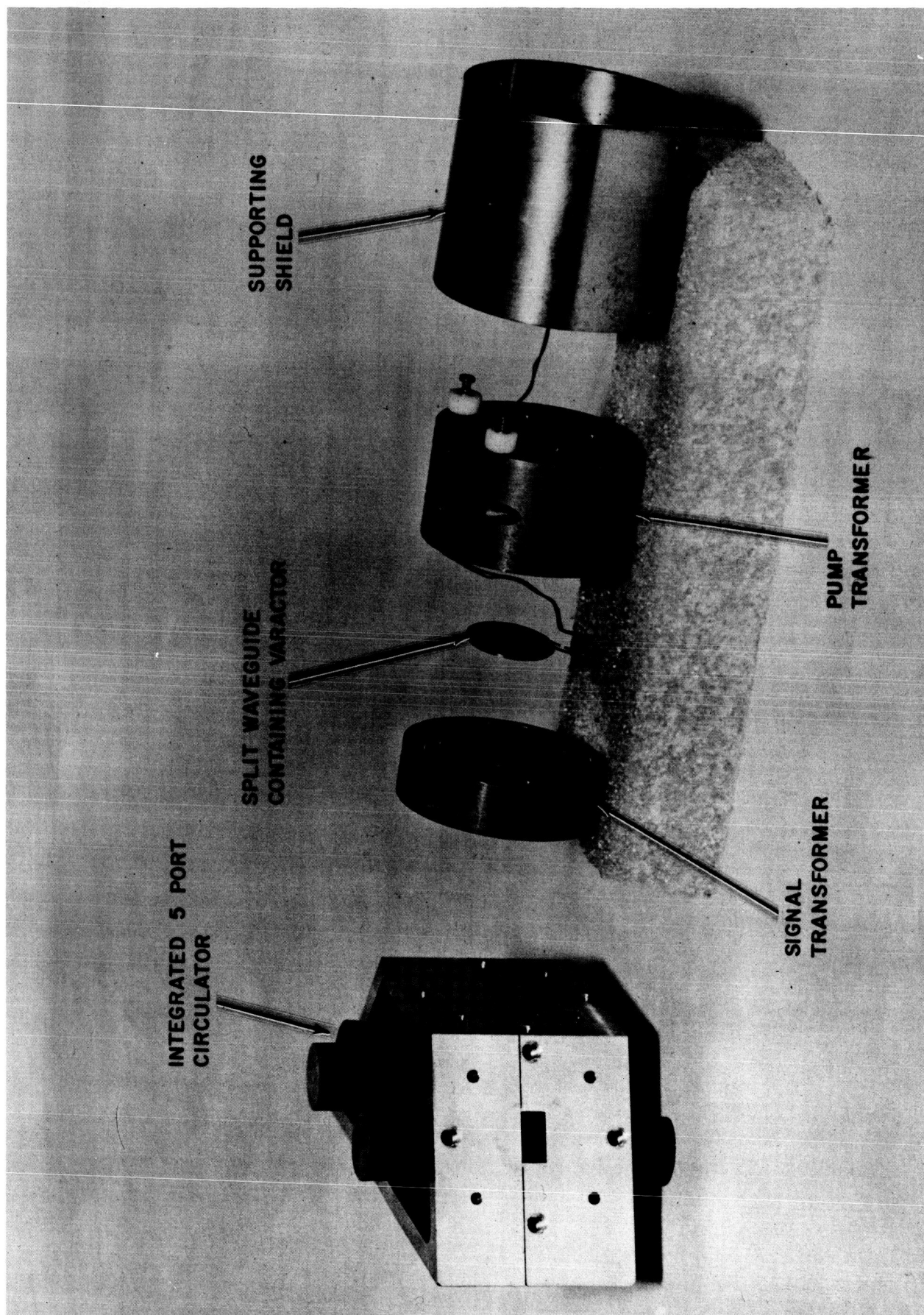


FIGURE 2 SINGLE DIODE AMPLIFIER

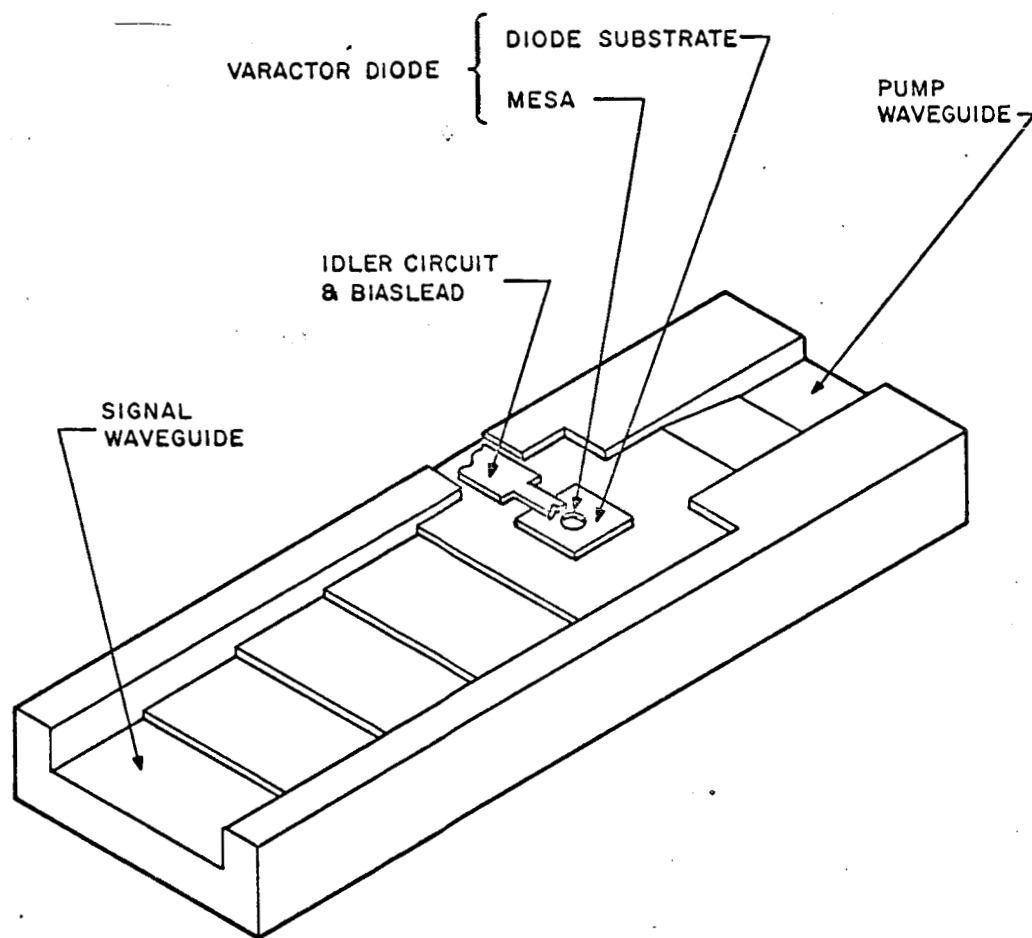


FIGURE 3 CUTAWAY VIEW OF 35 GC BALANCED
VARACTOR DIODE AMPLIFIER

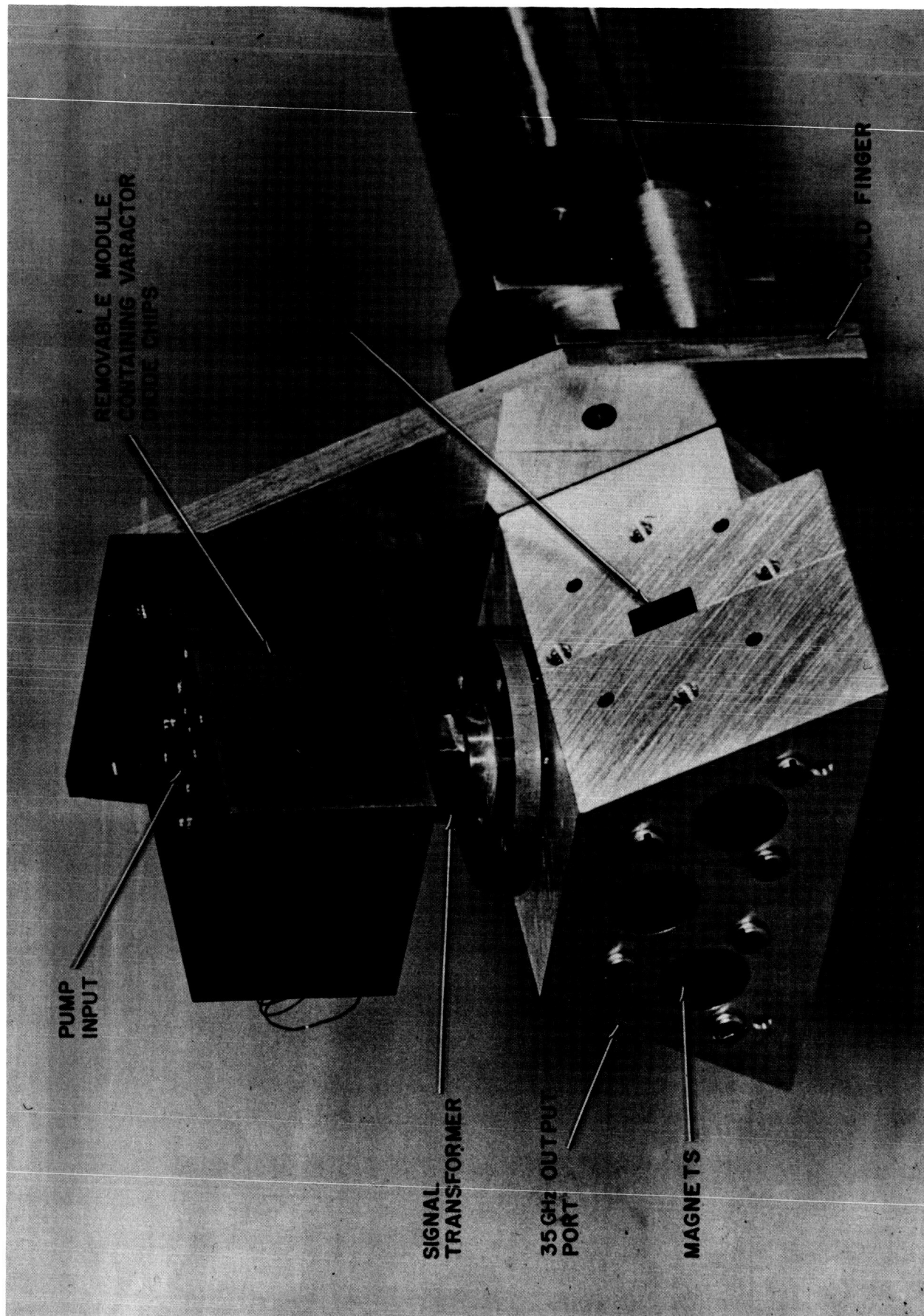


FIGURE 4 DETAILED VIEW OF BALANCED 35 GHz AMPLIFIER MOUNTED ON COLD FINGER

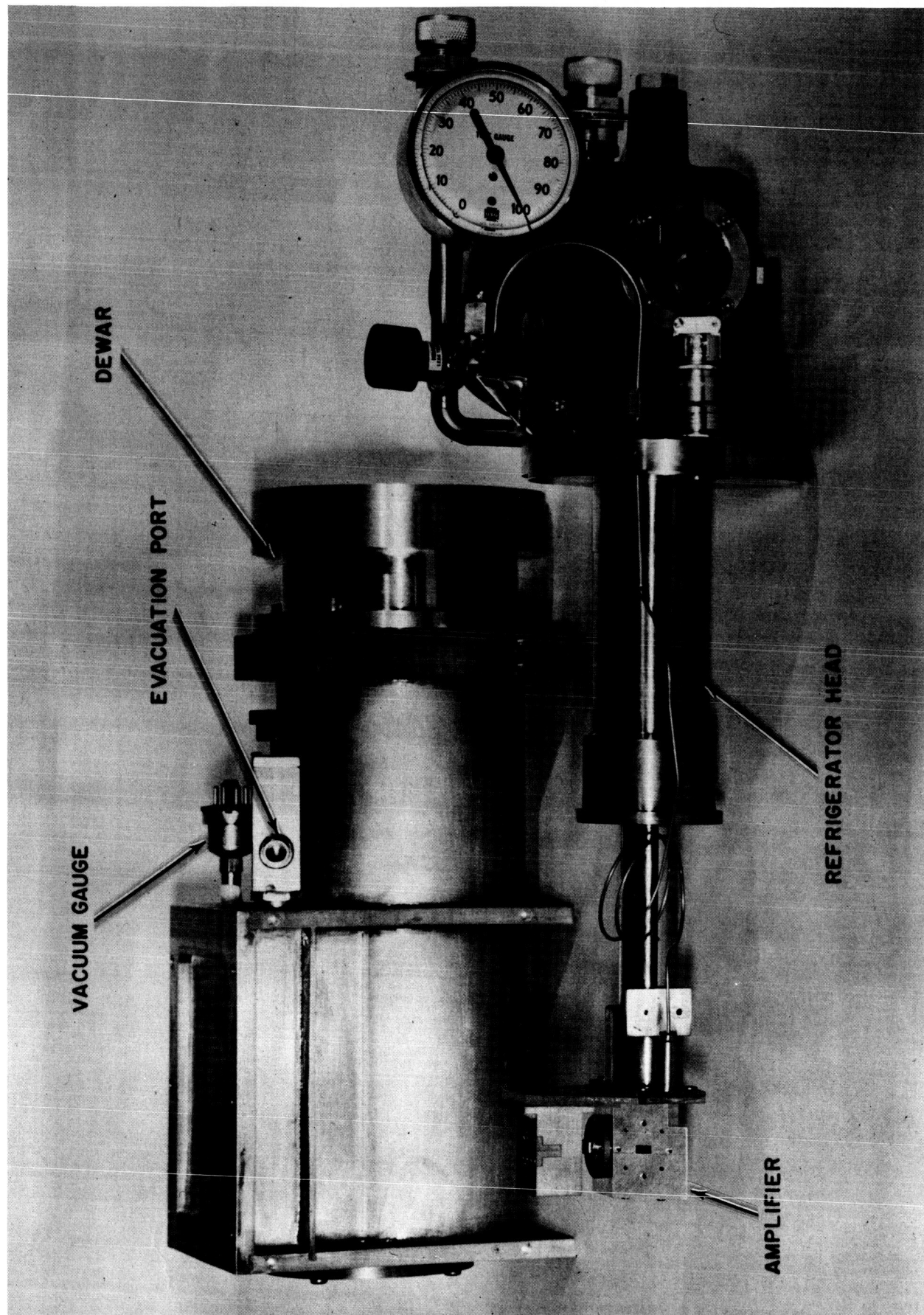


FIGURE 5 A. D. LITTLE REFRIGERATOR AND MATING TRG ALUMINUM DEWAR